Fig.1 (Prior Art)

(a)

Field	PID	ADDR	ENDP	CRC5
Bit	8	7	4	5

(b)

Field	PID	DATA	CRC16
Bit	8	0-8192	16

(c)

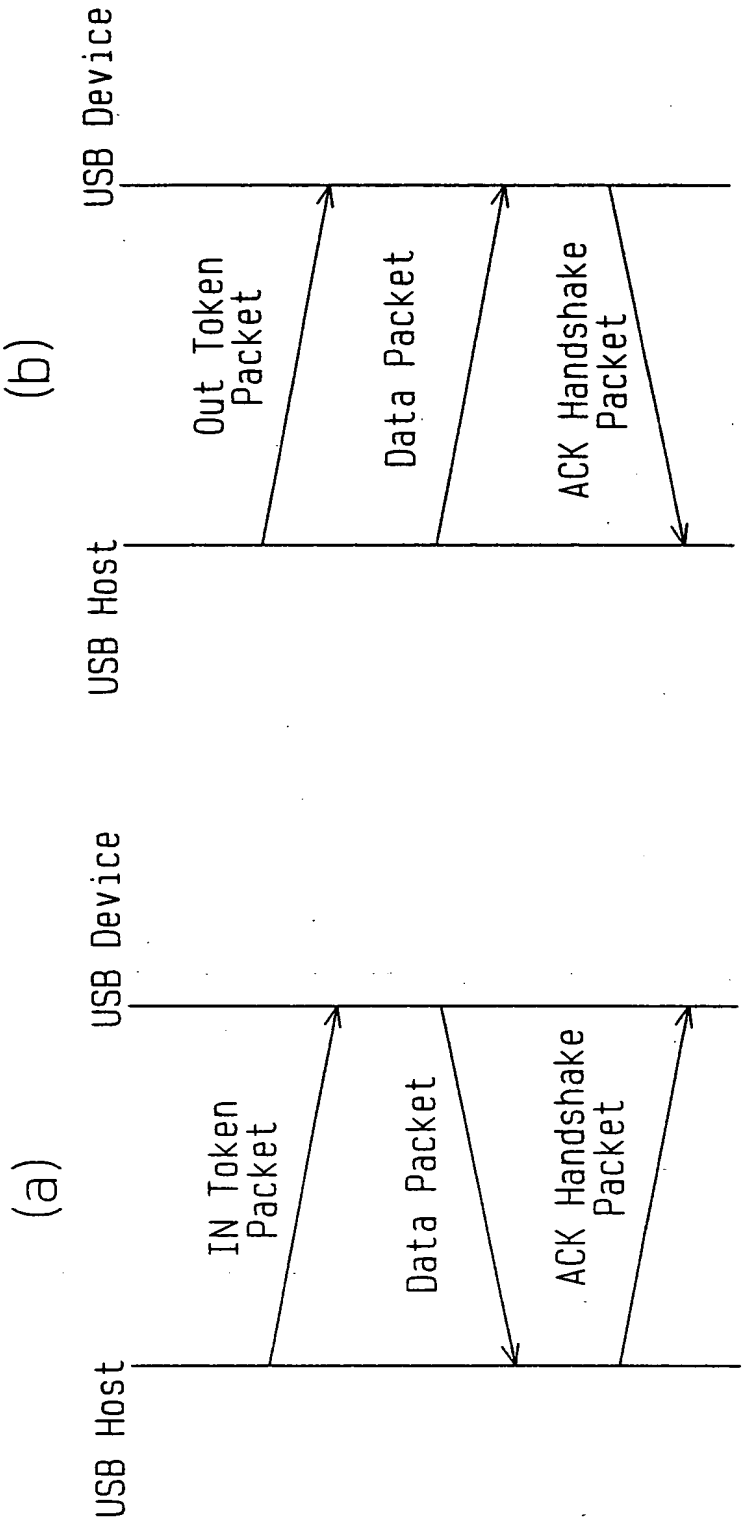
Field	PID
Bit	8

Fig.2 (Prior Art)

LSB MSB

PID0	PID1	PID2	PID3	$\overline{\text{PID0}}$	$\overline{\text{PID1}}$	$\overline{\text{PID2}}$	$\overline{\text{PID3}}$

Fig.3(Prior Art)



TITLE: DATA PROCESSOR, PACKET RECOGNITION METHOD, AND ERROR CORRECTION METHOD
INVENTORS: Kazuhiro AOSHIMA
SERIAL NO.: Unassigned
DOCKET NO.: 1076.1089

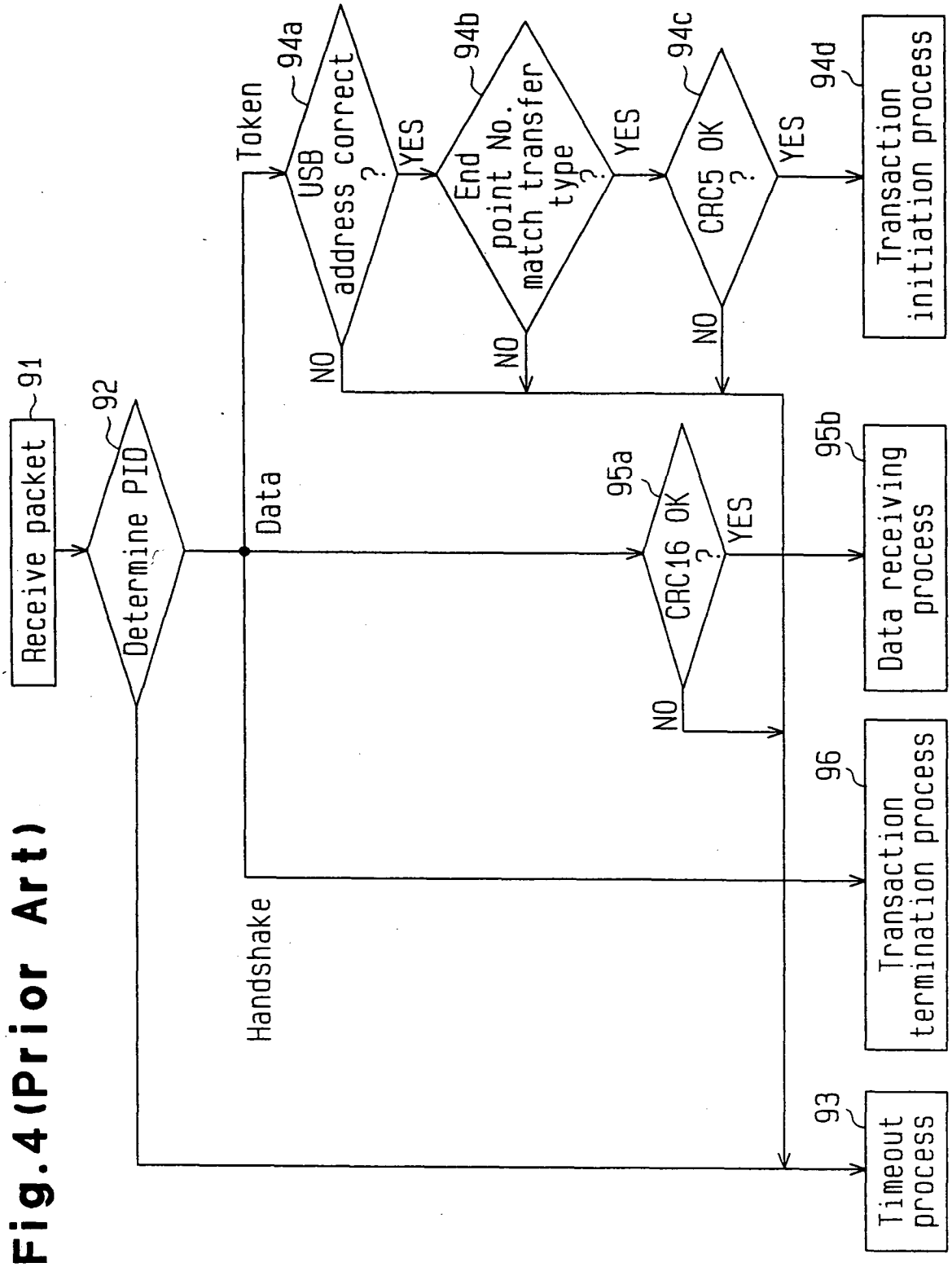


Fig.4(Prior Art)

Fig.5(Prior Art)

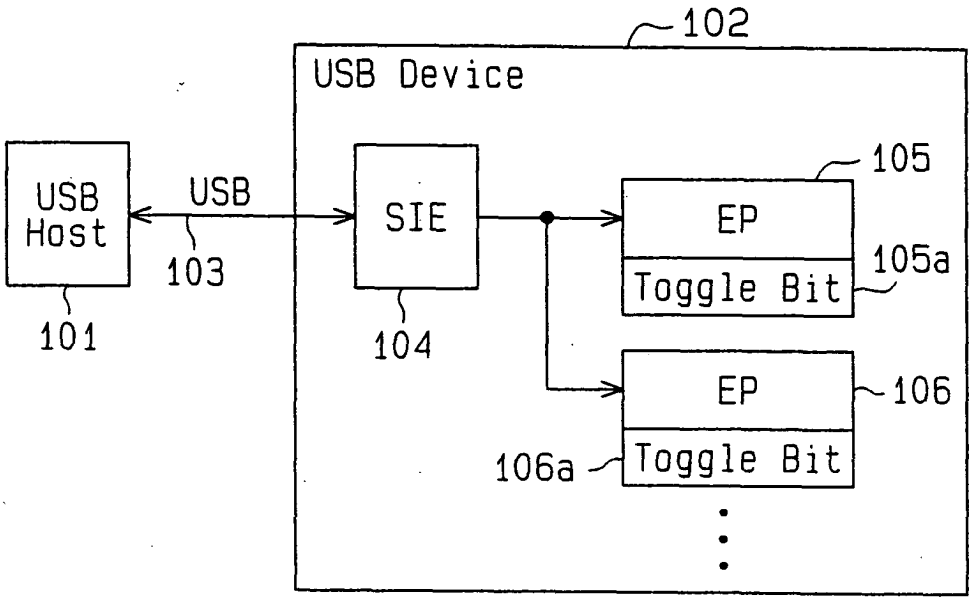
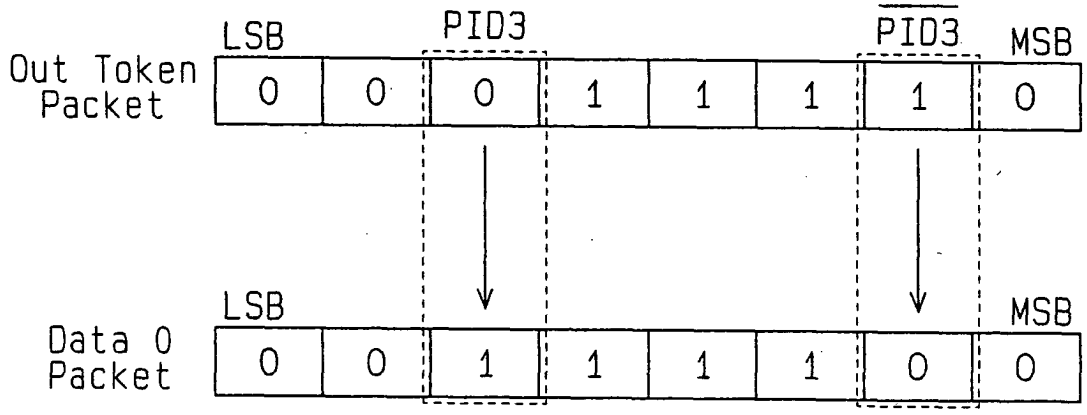


Fig.6(Prior Art)



TITLE: DATA PROCESSOR, PACKET RECOGNITION METHOD, AND ERROR CORRECTION METHOD
INVENTORS: Kazuhiro AOSHIMA
SERIAL NO.: Unassigned
DOCKET NO.: 1076.1089

Fig.7 (Prior Art)

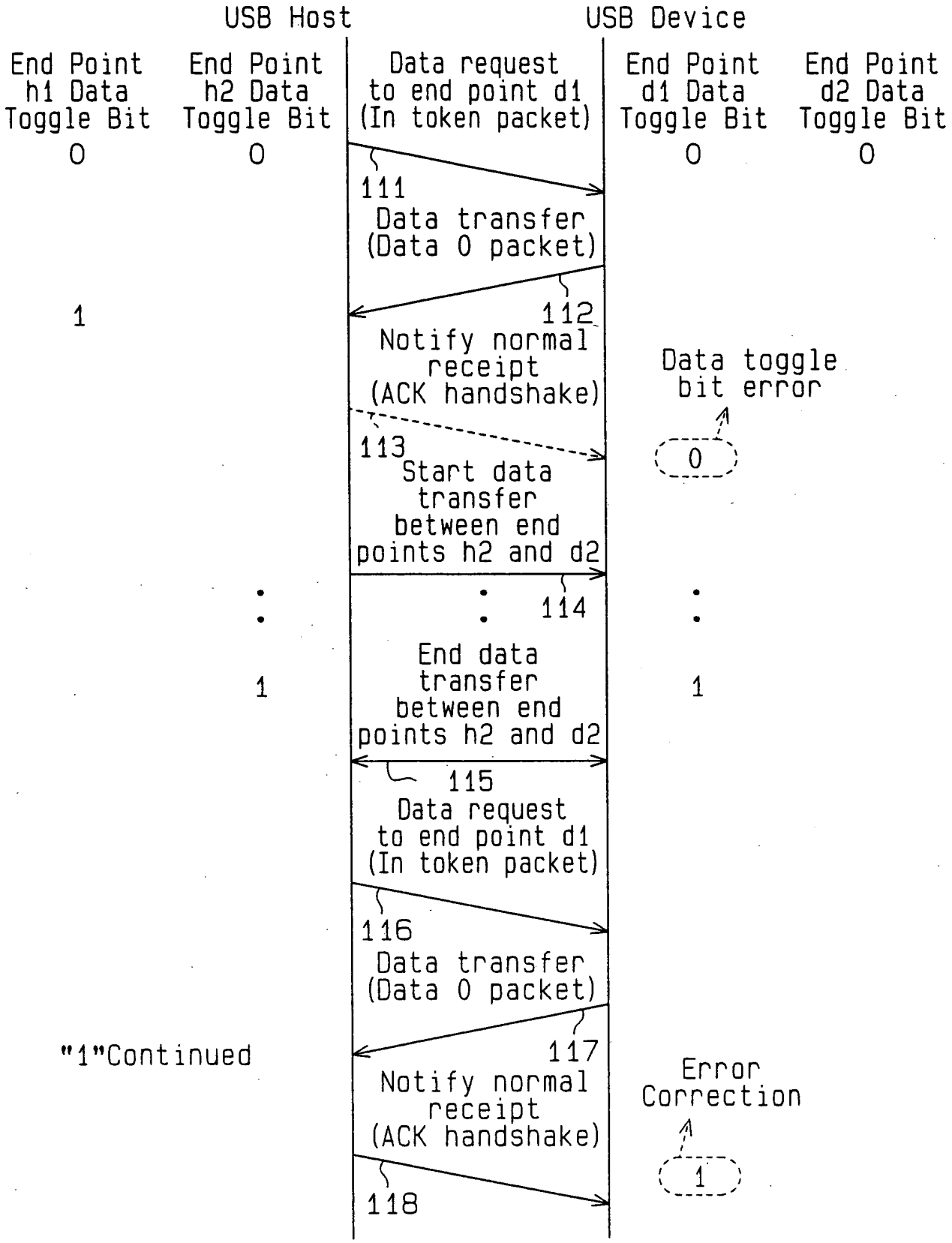


Fig.8

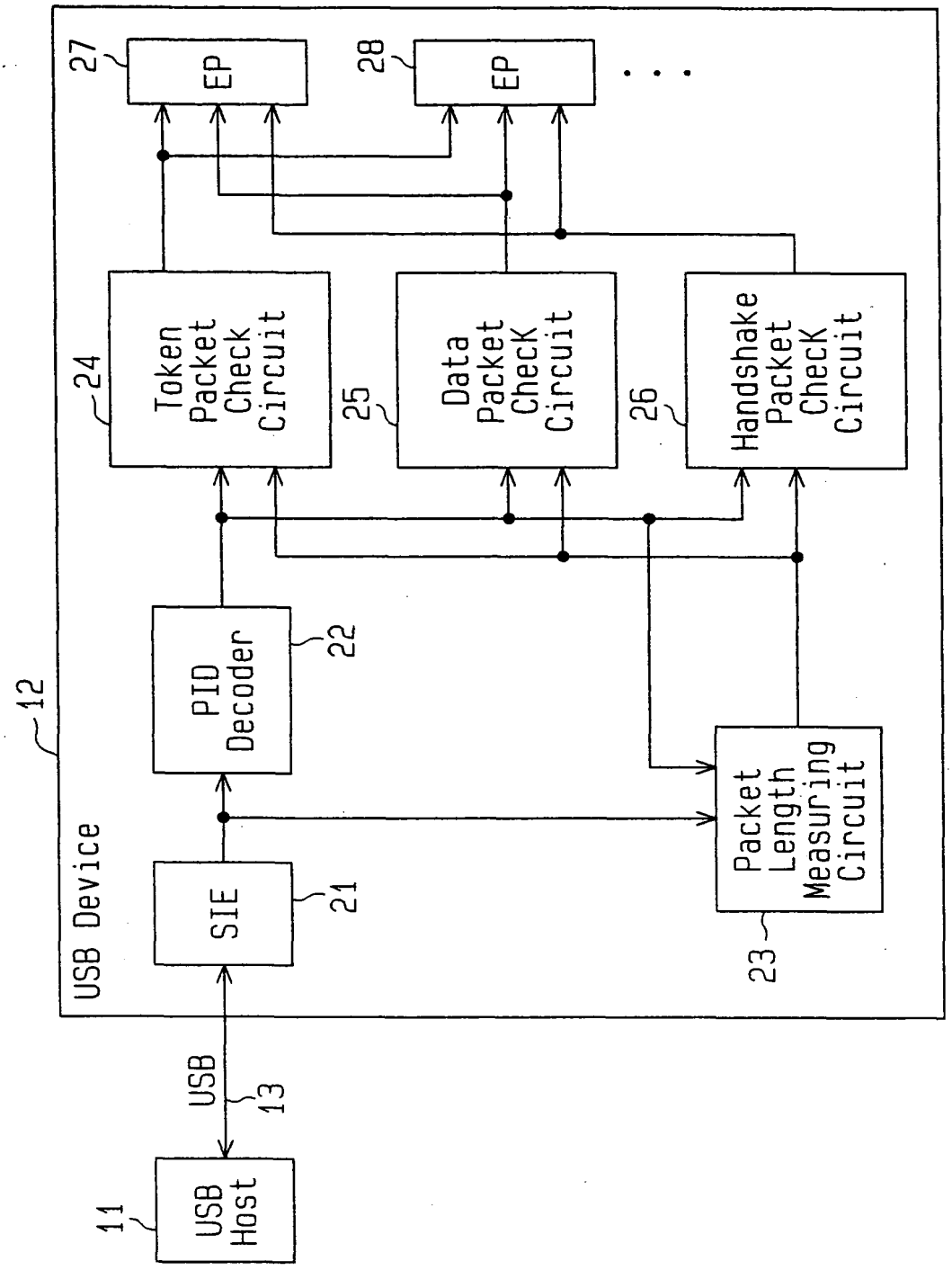

USB Device
12
27
EP
28
EP
24
Token Packet Check Circuit
25
Data Packet CheckK Circuit
26
Handshake Packet CheckK Circuit
PID Decoder
22
SIE
21
Packet Length Measuring Circuit
23
USB
13
USB Host
11

Fig.9

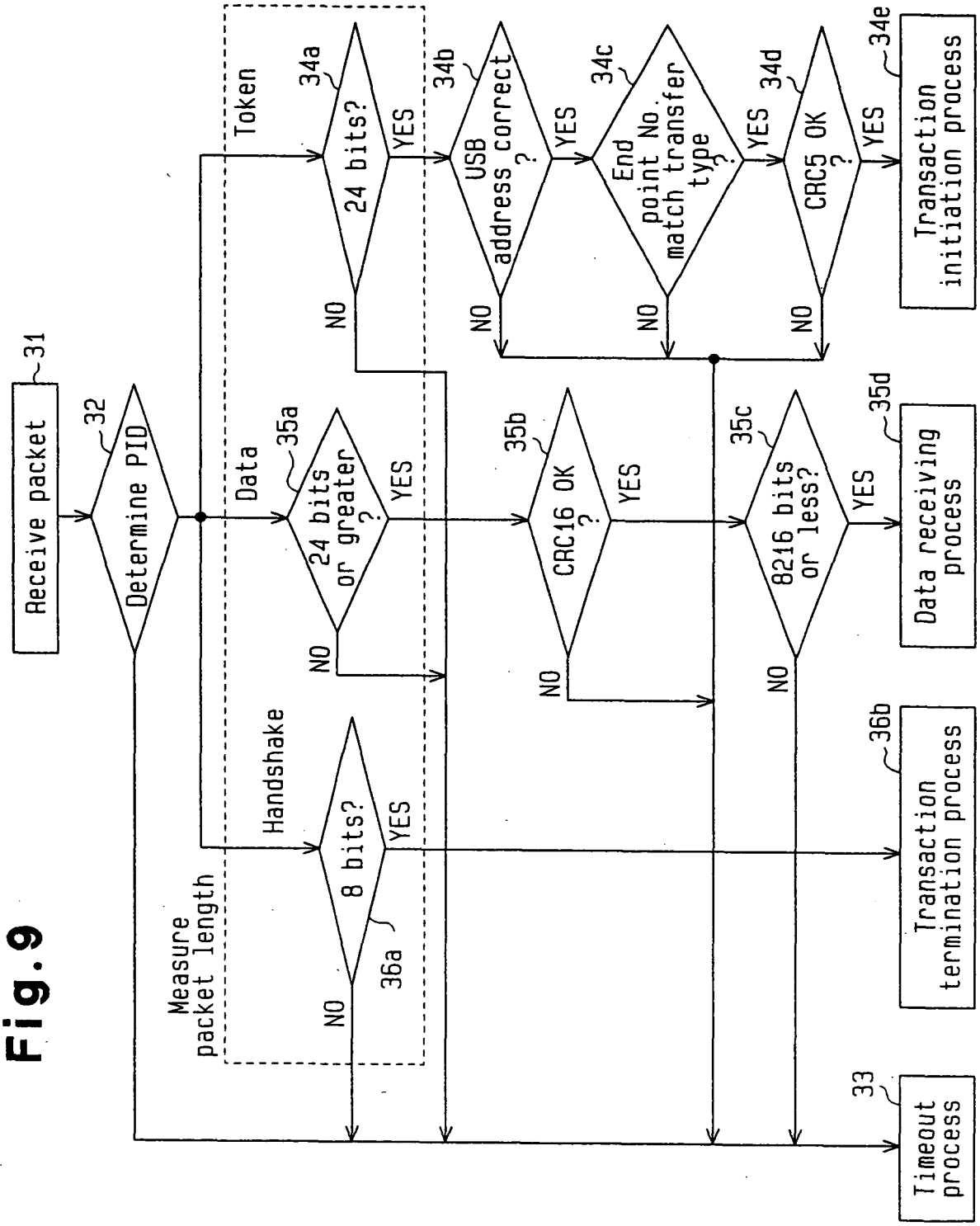

Receive packet
31
Determine PID
32
Token
Data
Handshake
Measure packet length
34a
24 bits?
YES
NO
34b
USB address correct ?
YES
NO
34c
End point No. match transfer type ?
YES
NO
34d
CRC5 OK ?
YES
NO
34e
Transaction initiation process
35a
24 bits or greater ?
YES
NO
35b
CRC16 OK ?
YES
NO
35c
8216 bits or less?
YES
NO
35d
Data receiving process
36a
8 bits?
YES
NO
36b
Transaction termination process
33
Timeout process

Fig.10

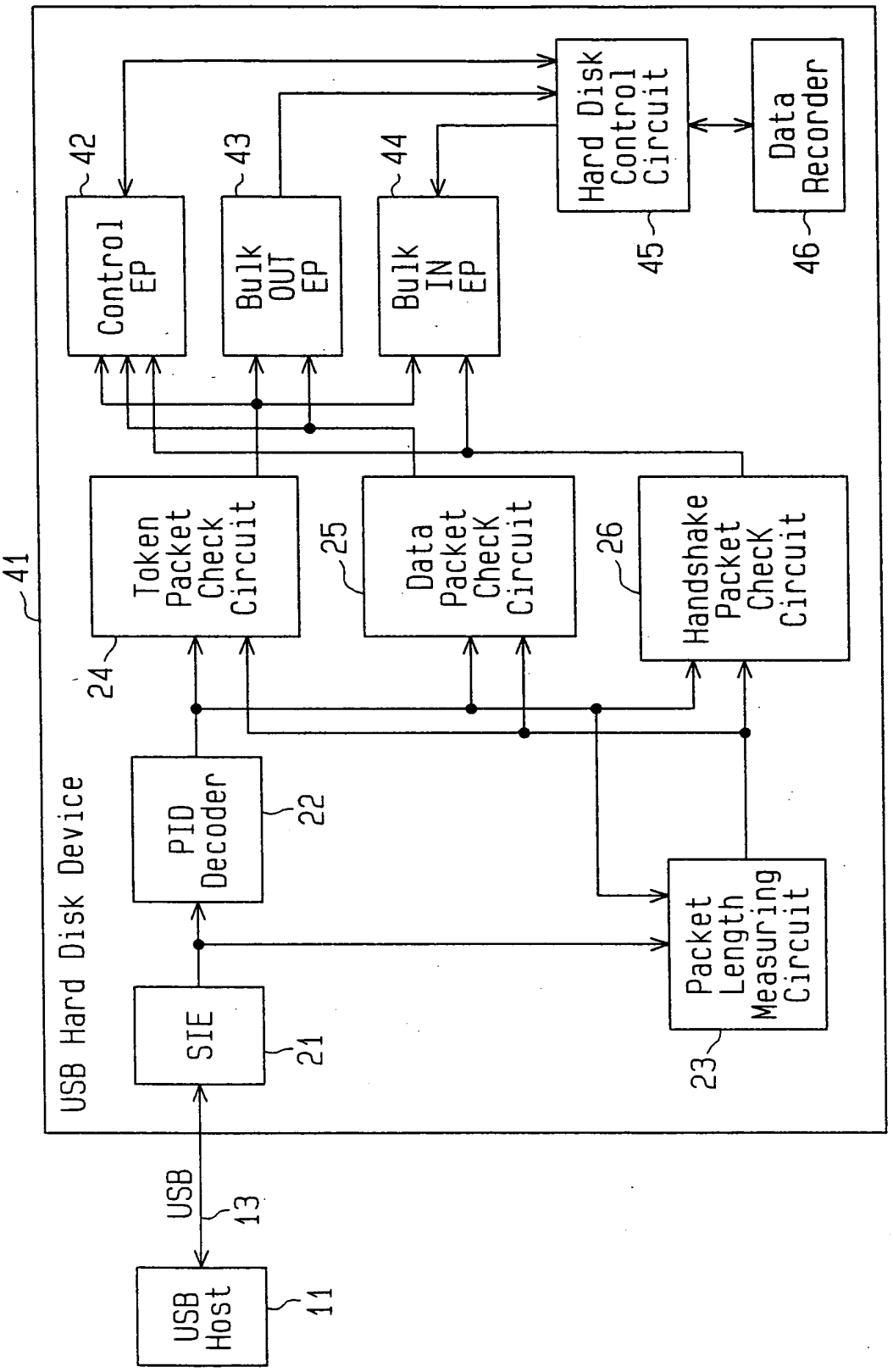

USB Hard Disk Device
41
Control EP
42
Bulk OUT EP
43
Bulk IN EP
44
Hard Disk Control Circuit
45
Data Recorder
46
Token Packet Check Circuit
24
Data Packet Check Circuit
25
Handshake Packet Check Circuit
26
PID Decoder
22
SIE
21
Packet Length Measuring Circuit
23
USB
13
USB Host
11

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Fig.11

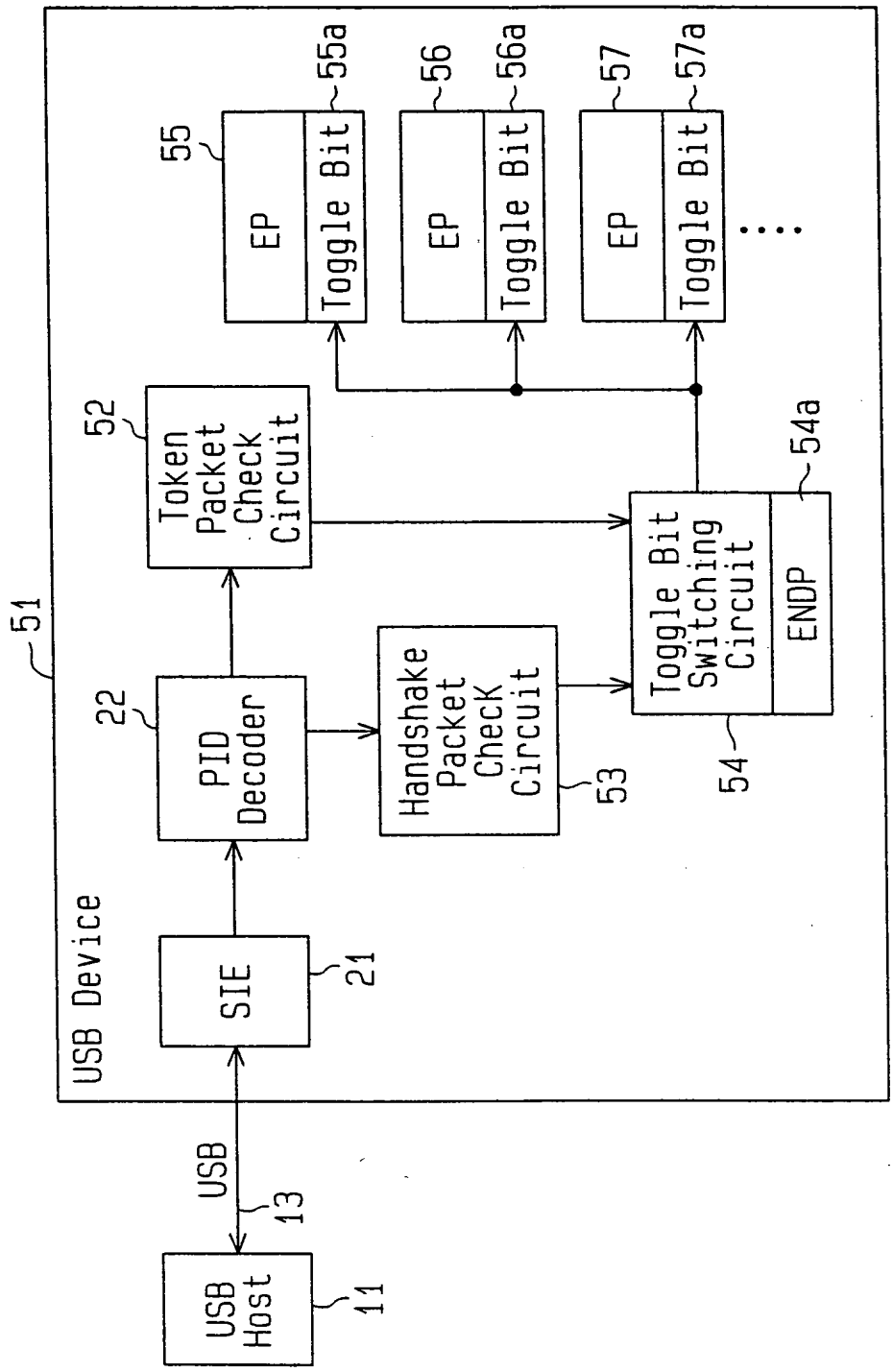


Fig.12

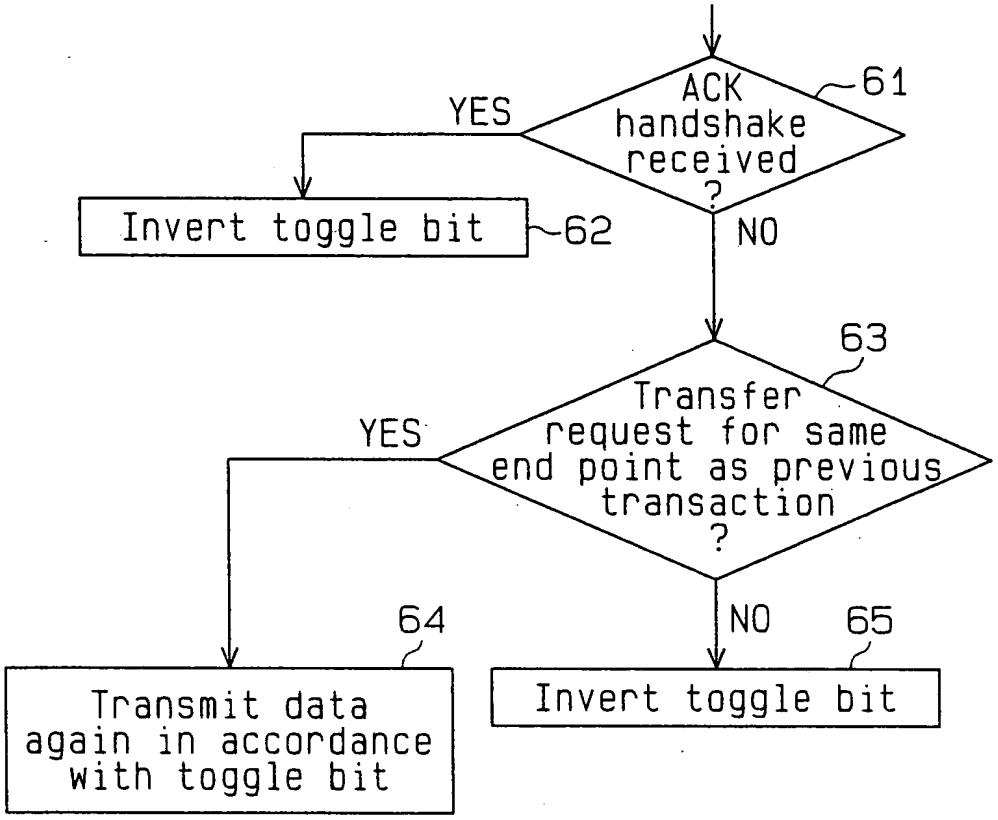

ACK handshake received ?
61
YES
Invert toggle bit
62
NO
63
Transfer request for same end point as previous transaction ?
YES
NO
64
65
Transmit data again in accordance with toggle bit
Invert toggle bit

Fig.13

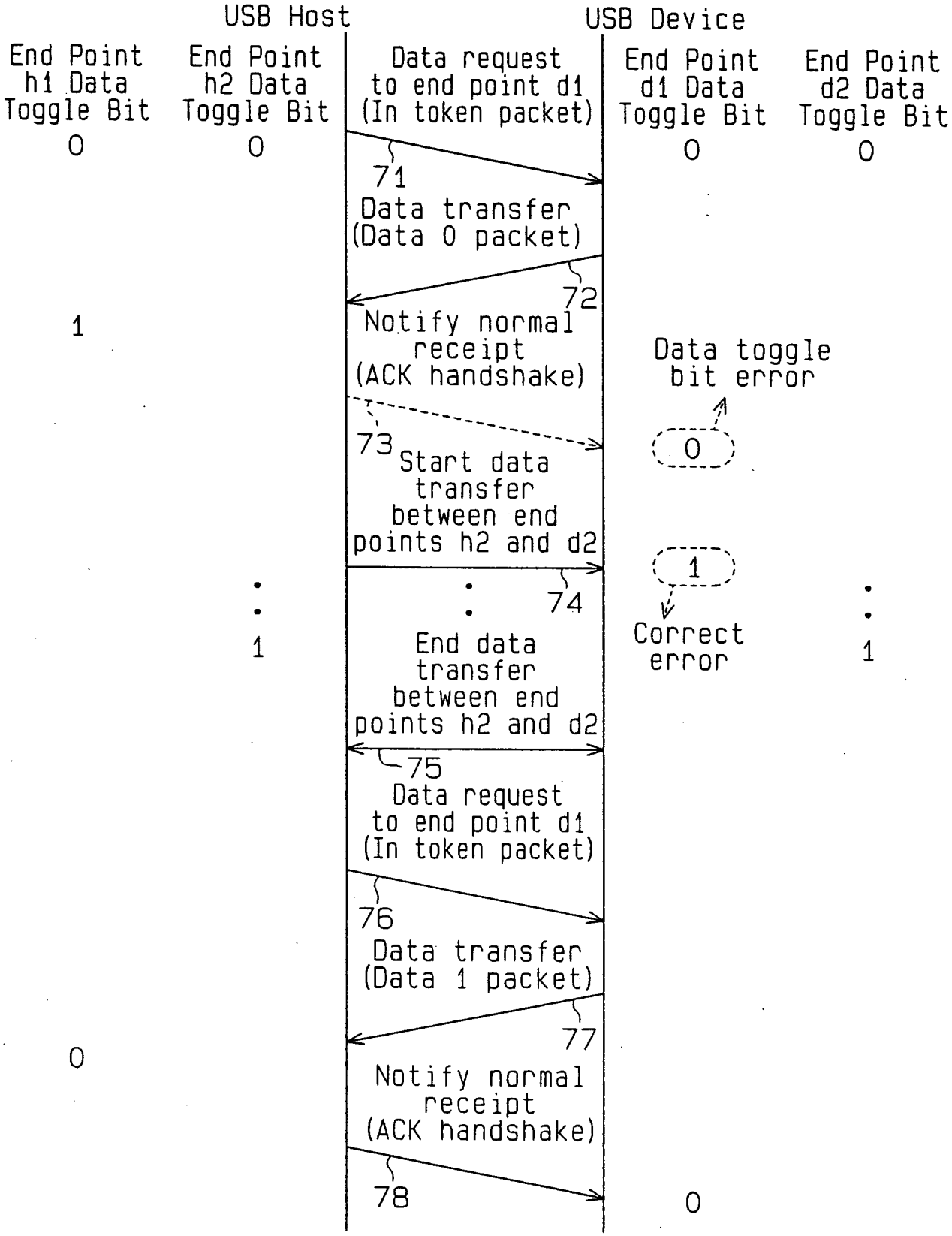
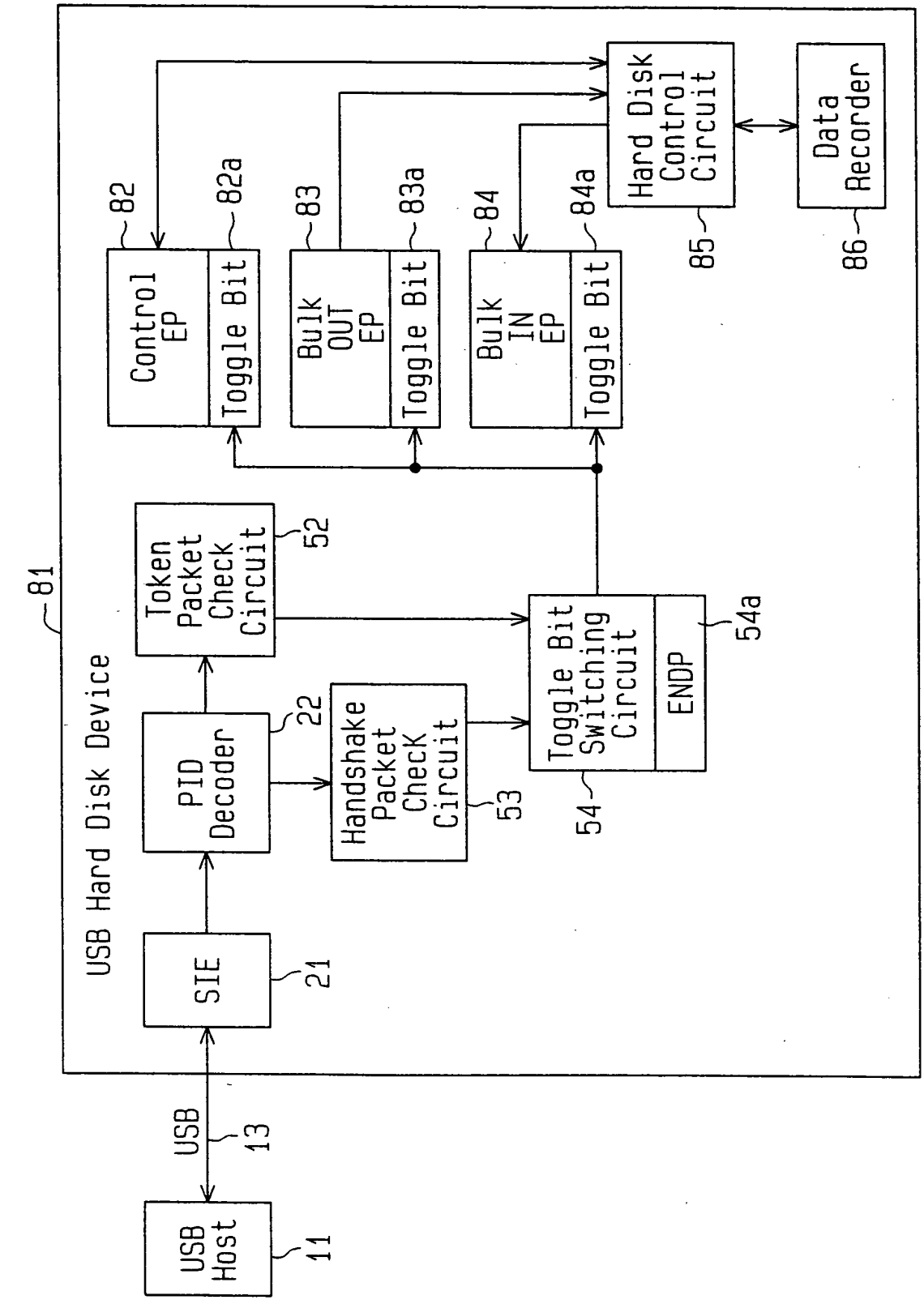

USB Host
USB Device
End Point h1 Data Toggle Bit
End Point h2 Data Toggle Bit
Data request to end point d1 (In token packet)
End Point d1 Data Toggle Bit
End Point d2 Data Toggle Bit
0
0
0
0
71
Data transfer (Data 0 packet)
72
1
Notify normal receipt (ACK handshake)
Data toggle bit error
73
0
Start data transfer between end points h2 and d2
1
74
1
1
End data transfer between end points h2 and d2
Correct error
75
Data request to end point d1 (In token packet)
76
Data transfer (Data 1 packet)
77
0
Notify normal receipt (ACK handshake)
78
0

Fig.14


USB Hard Disk Device
81
USB
13
USB Host
11
SIE
21
PID Decoder
22
Handshake Packet CheckK Circuit
53
Token Packet Check Circuit
52
Toggle Bit Switching Circuit
54
ENDP
54a
Control EP
82
Toggle Bit
82a
Bulk OUT EP
83
Toggle Bit
83a
Bulk IN EP
84
Toggle Bit
84a
Hard Disk Control Circuit
85
Data Recorder
86